What is claimed is:

1. A sub-block erase method of a non-volatile semiconductor memory device including a matrix of rows and columns of memory cells organized into more than one cell array block, wherein each said memory cell has a charge storage layer and a control gate stacked over each other through an insulative film above a semiconductor substrate and is set in any one of a write state with electrons injected into said charge storage layer and an erase state with electrons drawn out of said charge storage layer, wherein control gates of a plurality of memory cells aligned in a row direction are commonly connected together by a word line, and wherein a plurality of memory cells queued in a column direction are connected together by a bit line to thereby constitute a NAND cell unit, said method being for erasing more than one partial memory cell of said cell array block, said method comprising:

performing sub-block erase by giving a voltage for drawing electrons out of said charge storage layer to a control gate of said partial memory cell being an object to be erased;

performing sub-block erase verify read to check whether said memory cell to be erased is set in the erase state;

performing over-program verify read to check whether an over-programmed memory cell having its threshold voltage higher than a read voltage is present within said NAND cell unit;

when said sub-block erase verify read results in failure to make certain that said memory cell is in the erase state and when said over-programmed memory cell is absent, determining whether an execution number of said sub-block erase reaches a predefined allowable number, and then performing re-execution of said sub-block erase when the execution number does not reach the allowable number and

otherwise terminating the processing while regarding the erase as being inexecutable when the execution number reaches the allowable number;

determining the erase is completed to thereby terminate the processing when said memory cell to be erased becomes in the erase state during said sub-block erase verify read; and

determining the erase is inexecutable to thereby terminate the processing when an over-programmed memory cell is found to be present by said over-program verify read.

2. The method according to claim 1, wherein said sub-block erase verify read is performed prior to said over-program verify read.

3. The method according to claim 1, wherein said over-program verify read is done prior to said sub-block erase verify read.

4. The method according to claim 1, further comprising:

counting a number of NAND cell units each being determined by said over-program verify read to include therein an over-programmed memory cell; and

continuing the processing without rendering the erase inexecutable when the number as counted at this step is less than or equal to an error correctable number.

5. The method according to claim 1, further comprising:

counting a number of NAND cell units each being determined by said over-program verify read to include therein an over-programmed memory cell;

counting a number of NAND cell units being determined by said sub-block erase verify read to be incomplete in erase; and

virtually determining the erase is completed to thereby terminate the processing when a sum of these count values is less than or equal to an error correctable number.

6. The method according to claim 1, wherein the threshold voltage of said memory cell becomes a first threshold voltage higher than a ground potential and yet lower than the read voltage in the write state and is a second threshold voltage lower than the ground potential in the erase state,

said sub-block erase is done by giving the ground potential to the control gate of the memory cell to be erased and letting the bit line and control gates of memory cells other than the cell being erased be in an electrically floating state and then applying a high voltage to the semiconductor substrate,

said over-program verify read is done by applying the read voltage to the control gates of all the memory cells, and

said sub-block erase verify read is done by applying the ground potential to the control gate of the memory cell to be erased while applying the read voltage to the control gates of the other memory cells.

7. The method according to claim 6, wherein said over-program verify read and said sub-block erase verify read are continuously executed by merely changing an applied voltage to the control gate of the memory cell to be erased.

8. A nonvolatile semiconductor memory device comprising:

a memory cell array with a matrix of rows and columns of memory cells organized into more than one cell array block, wherein each said memory cell has a charge storage layer and a control gate stacked over each other through an insulative film above a semiconductor substrate and is set in any one of a write state with electrons injected into said charge storage layer and an erase state with electrons drawn out of said charge storage layer, and wherein control gates of a plurality of memory cells aligned in a row

direction are commonly connected together by a word line, and wherein a plurality of memory cells queued in a column direction are connected together by a bit line to thereby constitute a NAND cell unit;

control means for applying to this memory cell array certain voltages for execution of write and read of said memory cell and also of sub-block erase for erasing more than one partial memory cell of said cell array block; and

said control means including,

means for performing sub-block erase by giving a voltage for drawing electrons out of said charge storage layer to a control gate of said partial memory cell being an object to be erased;

means for performing sub-block erase verify read to check whether said memory cell to be erased is set in the erase state;

means for performing over-program verify read to check whether an over-programmed memory cell having its threshold voltage higher than a read voltage is present within said NAND cell unit;

means for determining, when said sub-block erase verify read results in failure to affirm that said memory cell is in the erase state and when said over-programmed memory cell is absent, whether an execution number of said sub-block erase reaches a predefined allowable number and for permitting re-execution of said sub-block erase when the execution number does not reach the allowable number and otherwise terminating the processing while regarding the erase as being inexecutable when the execution number reaches the allowable number;

means for determining the erase is completed to thereby terminate the processing when said memory cell to be erased becomes in the erase state during said sub-block erase verify read; and

means for determining the erase is inexecutable to thereby terminate the processing when an over-programmed memory cell is found to be present by said over-program verify read.

9. An electric card equipped with a non-volatile semiconductor memory device defined in claim 8.

10. An electric device comprising:

a card interface;

a card slot connected to said card interface; and

an electric card defined claim 9 and electrically connectable to said card slot.

11. The electric device according to claim 10, wherein said electric device is a digital still camera.